IN THE SPECIFICATION

Please replace the paragraph at page 4, lines 7-10, with the following rewritten paragraph:

Further, when pixel data are written in the GRAM 2, the memory clock signal 53 is fed to the GRAM 2. ~~When~~ and the memory clock signal 53 falls~~, pixel data are written in the GRAM 2~~. In this manner, the pixel data are written in the GRAM 2 in synchronization to the memory clock signal 53.

Please replace the paragraph at page 13, line 5, to page 14, line 1, with the following rewritten paragraph:

The 1st aspect of the present invention is a video signal processing circuit, comprising:

a GRAM which stores pixel data, which is data corresponding to pixels of a display screen, at least in the amount equivalent to said display screen, said pixel data being written in said GRAM in synchronization to a memory clock signal;

a latch circuit which reads and stores pixel data corresponding to pixels representing a scanning line of said display screen from said GRAM; and

a control ~~means~~ unit,

wherein said pixel data corresponding to said pixels representing said scanning line stored in said latch circuit is displayed on said display screen, and

in the case of contention between writing of said pixel data in said GRAM and reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM, said control ~~means~~ unit delays for a predetermined delay time reading of said pixel data corresponding to said pixels representing said scanning line and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again.

Please replace the paragraph at page 14, lines 2-12, with the following rewritten paragraph:

The 2nd aspect of the present invention is the video signal processing circuit of the 1st aspect of the present invention, wherein said control ~~means~~ unit comprises a delay ~~means~~ unit which delays and inputs a display read control signal and a data latch signal for said predetermined delay time during a period which is after a point at which said memory clock signal corresponding to writing of said pixel data in said GRAM is supplied, said writing accompanying said contention, but which is before supplying of the next memory clock signal following said memory clock signal so that said latch circuit reads pixel data corresponding to pixels representing said scanning line.

Please replace the paragraph at page 14, lines 13-15, with the following rewritten paragraph:

The 3rd aspect of the present invention is the video signal processing circuit of the 2nd aspect of the present invention, wherein said predetermined delay time can be adjusted in a variable manner.

Please replace the paragraph at page 14, lines 16-22, with the following rewritten paragraph:

The 4th aspect of the present invention is the video signal processing circuit of the 1st aspect of the present invention, wherein said control ~~means~~ unit comprises a monitoring ~~means~~ unit which monitors whether writing of said pixel data in said GRAM contends against reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM.

Please replace the paragraph at page 14, line 23, to page 15, line 6, with the following rewritten paragraph:

The 5th aspect of the present invention is the video signal processing circuit of the 4th aspect of the present invention, wherein said control ~~means~~ unit comprises a delay ~~means~~ unit which delays reading of said pixel data corresponding to said pixels representing said scanning line based on a monitoring result obtained by said monitoring ~~means~~ unit and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM once again.

Please replace the paragraph at page 15, lines 7-20, with the following rewritten paragraph:

The 6th aspect of the present invention is the video signal processing circuit of the 1st aspect of the present invention, wherein when writing of said pixel data in said GRAM is executed plural times during a contention-free memory update period in which said pixel data corresponding to said pixels representing said scanning line are read to said latch circuit from said GRAM said control ~~means~~ unit upon occurrence of said contention delays reading of said pixel data corresponding to said pixels representing said scanning line between a period of writing said pixel data and a period of writing next pixel data, and controls so as to perform reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM again plural times during said contention-free memory update period.

Please replace the paragraph at page 15, line 21, to page 16, line 12, with the following rewritten paragraph:

The 7th aspect of the present invention is a method of controlling a video signal processing circuit which comprises:

a GRAM which stores pixel data, which is data corresponding to pixels of a display screen, at least in the amount equivalent to said display screen, said pixel data being written in said GRAM in synchronization to a memory clock signal;

a latch circuit which reads and stores pixel data corresponding to pixels representing a scanning line of said display screen from said GRAM; and

a control ~~means~~ unit,

said method comprising a step at which in the case of contention between writing of said pixel data in said GRAM and reading of said pixel data corresponding to said pixels representing said scanning line to said latch circuit from said GRAM, said control ~~means~~ unit delays for a predetermined delay time reading of said pixel data corresponding to said pixels representing said scanning line.

Please replace the paragraph at page 17, line 23, with the following rewritten paragraph:

4 latch circuit control ~~means~~ unit

Please replace the paragraph at page 18, line 20, to page 19, line 2, with the following rewritten paragraph:

The video processing circuit 1 comprises a latch circuit 3, a GRAM (graphics Random access memory) 2 and a control ~~means~~ unit 4. The GRAM 2 is a readable/writable memory which stores pixel data amounting to one screen displayed by a display panel 8, and

in this memory, pixel data corresponding to one pixel which forms the display panel 8 is written in synchronization to a memory clock signal 12 which is input.

Please replace the paragraph at page 19, lines 6-12, with the following rewritten paragraph:

The control ~~means~~ unit 4 is a circuit which generates a control signal, which controls so that pixel data equivalent to one scanning line will be read again from the GRAM 2 to the latch circuit 3 upon occurrence of contention between writing of pixel data in the GRAM 2 and reading of pixel data equivalent to one scanning line to the latch circuit 3 from the GRAM 2, and outputs the control signal to the latch circuit 3.

Please replace the paragraph at page 19, lines 13-15, with the following rewritten paragraph:

The control ~~means~~ unit 4 comprises a delay circuit 7, an OR circuit 5, an OR circuit 6, a delay time storage memory 91 and a monitoring circuit 92.

Please replace the paragraph at page 20, lines 12-14, with the following rewritten paragraph:

The delay circuit 7 and the delay time storage memory 91 according to this embodiment is an example of the delay ~~means~~ unit of the present invention.

Please replace the paragraph at page 20, lines 17-20, with the following rewritten paragraph:

The display read control signal 9, the data latch signal 10 and the memory clock signal 12 are input to the control ~~means~~ unit 4. Meanwhile, the memory clock signal 12 is input to the GRAM 2.

Please replace the paragraph at page 23, lines 1-4, with the following rewritten paragraph:

Further, when pixel data are written in the GRAM 2, the memory clock signal 12 is fed to the GRAM 2~~. When~~ and the memory clock signal 12 falls~~, pixel data are written in the GRAM 2~~. In this manner, the pixel data are written in the GRAM 2 in synchronization to the memory clock signal 12.

Please replace the paragraph at page 27, line 22, to page 28, line 8, with the following rewritten paragraph:

That is, the delay circuit 7 of the control ~~means~~ unit 4 receives the memory clock signal 16 and delays the memory clock signal 16 by a predetermined time, generates the display read control for host retry 17 and the data latch signal for host retry 18, and outputs these respectively to the OR circuit 6 and the OR circuit 5. The predetermined time above is determined based on information which is indicative of a delay time which is stored in the delay time storage memory 91. Also set in advance by a command within the delay time storage memory 91 is information indicative of the delay time. It is possible to set the information indicative of the delay time once again by a command.

Please replace the paragraph at page 29, lines 9-25, with the following rewritten paragraph:

In the case of contention between writing of pixel data in the GRAM 2 and reading of pixel data representing one scanning line to the latch circuit 3 from the GRAM 2, the control ~~means~~ unit 4 delays the discharge period, the memory update period and the timing of finalizing data, starting at the memory clock signal 16 at which the contention has occurred, by a predetermined time which is based on the information indicative of the delay time stored in the delay time storage memory 91, as denoted at the upon-contention display read control signal 19 and the upon-contention data latch signal 20. Hence, even despite contention between writing of pixel data in the GRAM 2 and reading of pixel data from the GRAM 2 to the latch circuit 3, the latch circuit 3 can execute re-reading while the display read control signal 9 is in the memory update period, and therefore, it is possible to read normally pixel data representing one scanning line from the GRAM 2 to the latch circuit 3.

Please replace the paragraph at page 32, lines 20-22, with the following rewritten paragraph:

The delay circuit 7 and the delay time storage memory 91 according to the second embodiment is an example of the delay ~~means~~ unit of the present invention.

Please replace the paragraph at page 38, lines 2-7, with the following rewritten paragraph:

Noting this, in this case, the delay circuit 7 of the control ~~means~~ unit 4 receives the memory clock signal 12 and delays the memory clock signal 12 by a predetermined time, generates the display read control for host retry 26 and the data latch signal for host retry 27, and outputs these respectively to the OR circuit 6 and the OR circuit 5.

Please replace the paragraph at page 39, lines 7-23, with the following rewritten paragraph:

In the case of contention between writing of pixel data in the GRAM 2 and reading of pixel data representing one scanning line from the GRAM 2 to the latch circuit 3, the control ~~means~~ unit 4 delays the discharge period, the memory update period and the timing of finalizing data by a predetermined time, starting at the memory clock signal 16 at which the contention has occurred, as denoted at the upon-contention display read control signal 28 and the upon-contention data latch signal 29. Under the control of the control ~~means~~ unit 4, the discharge period and the memory update period start and feeding of the new upon-contention data latch signal 29 to the latch circuit 3 ends before the GRAM 2 receives the next memory clock signal 25 following the contention-bearing memory clock signal 25. This control is attained easily, as information indicative of a time which is based on the cycle of the memory clock signal 12 is set as the information indicative of the delay time stored in the delay time storage memory 91.

Please replace the paragraph at page 41, lines 16-21, with the following rewritten paragraph:

Further, although the foregoing has described that the latch circuit 3 reads and stores pixel data equivalent to one scanning line on the display panel [[2]] 8 from the GRAM 2 according to the second embodiment, this is not limiting. The latch circuit 3 may read and store pixel data equivalent to plural scanning lines from the GRAM 2.

Please replace the paragraph at page 45, lines 6-11, with the following rewritten paragraph:

Upon occurrence of this, the delay circuit 7 of the control ~~means~~ unit 4 receives the memory clock signal 12 and delays the memory clock signal 12 by a predetermined time, generates the display read control for host retry 84 and the data latch signal for host retry 85, and outputs these respectively to the OR circuit 6 and the OR circuit 5.

Please replace the paragraph at page 46, line 25, to page 47, line 16, with the following rewritten paragraph:

In the case of contention between writing of pixel data in the GRAM 2 and reading of pixel data representing one scanning line from the GRAM 2 to the latch circuit 3, the control ~~means~~ unit 4 delays the discharge period, the memory update period and the timing of finalizing data by a predetermined time, starting at the memory clock signal 83 at which the contention has occurred, as denoted at the upon-contention display read control signal 86 and the upon-contention data latch signal 87. Under the control of the control ~~means~~ unit 4, the new discharge period and the new memory update period start and feeding of the new upon-contention data latch signal 87 to the latch circuit 3 ends before the GRAM 2 receives the next memory clock signal 83 following the contention-bearing memory clock signal 83. In the third embodiment, this control is exercised the number of times that the memory clock signal 83 becomes the H-state while the normal-time display read control signal 81 is in the memory update period.

Please replace the Abstract at page 53, lines 1-15, with the following rewritten Abstract: